KBOC BASEBOARD#2 USER INFORMATION

KBOC_BB2_USER.PDF
KwikByte, LLC

Version 1.0

Revision Information

Revision	Date	Description
1.0	10/15/2009	Initial creation

DISCLAIMER

The KBOC_BB2 is an evaluation board intended for use in engineering development or demonstration and is not considered a final, end-item production unit. The device generates and uses radio frequency energy and has not been tested for compliance with FCC rules part 15. Use and operation of this device may cause radio interference – in which case the user must take corrective action at his own expense. In most cases, this simply involves discontinuing use of the device in that particular environment. Manufacturer is under no obligation to continue to produce this equipment for any length of time. This product is not intended for use in life-sustaining or life-critical systems. This product is not intended for use in nuclear devices. Appropriate ESD handling precautions must be taken when handling the device.

1 Introduction

The KBOC BASEBOARD#2 is intended for use as a hardware interface to the OMAP35xx-based KBOC System Module. This document provides important information about the KBOC BASEBOARD#2 ("KBOC_BB2") including physical dimensions, connector location and pin-out, and peripheral signal routing.

1.1 Physical Details

The figure below shows the KBOC_BB2 physical dimensions (5.00" x 4.00") and connector placement.

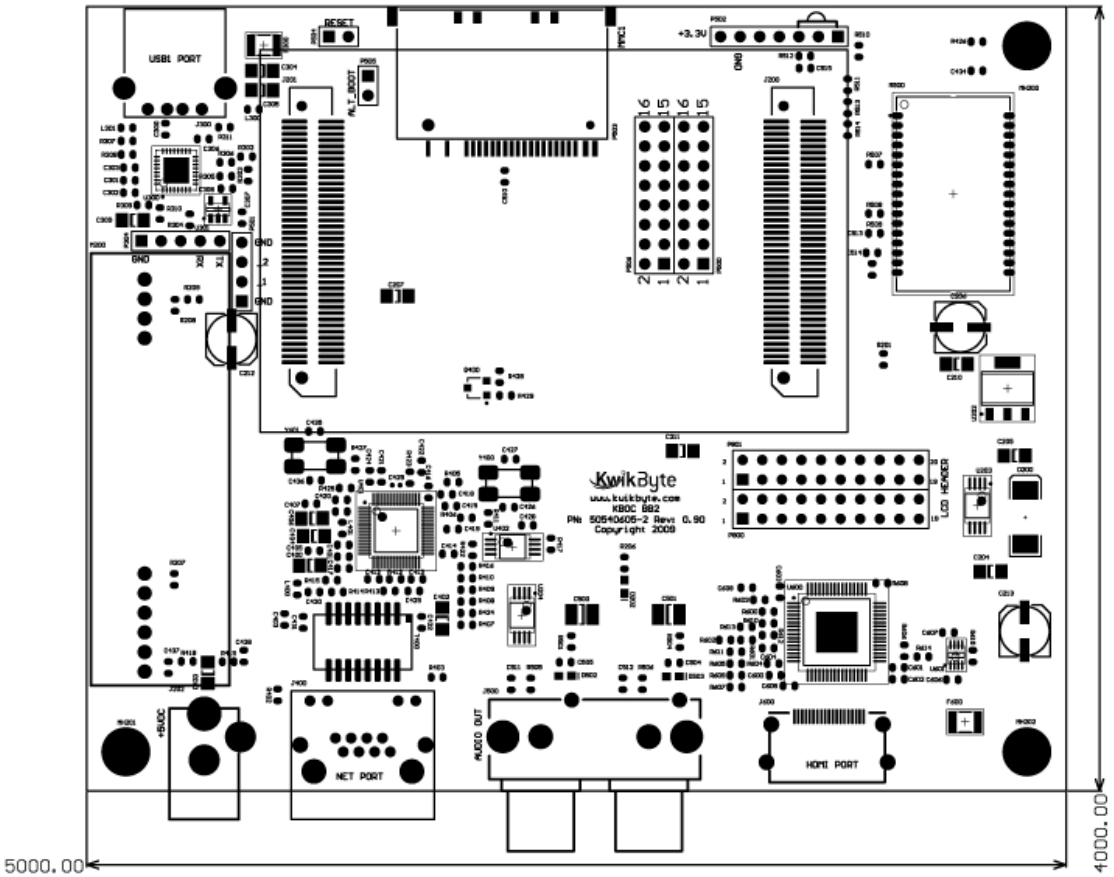

Figure 1-1: KBOC_BB2 DIMENSIONS

The three mount holes are positioned 0.200" back from each edge, at the corner, and drilled at 0.140" diameter.
The figures below depict 3D images of the board viewed from top and connector edges. Note: some components shown are populated depending on configuration and may not be installed on a specific board.

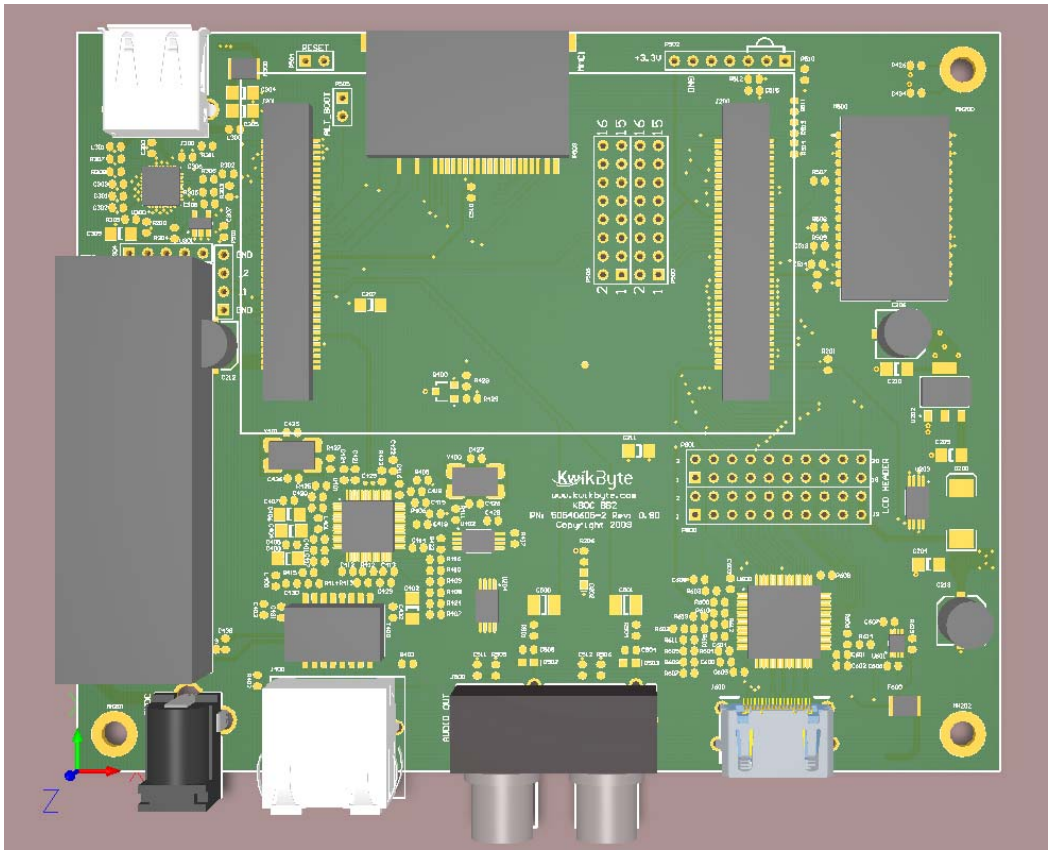

Figure 1-2: KBOC_BB2 3D VIEW FROM TOP

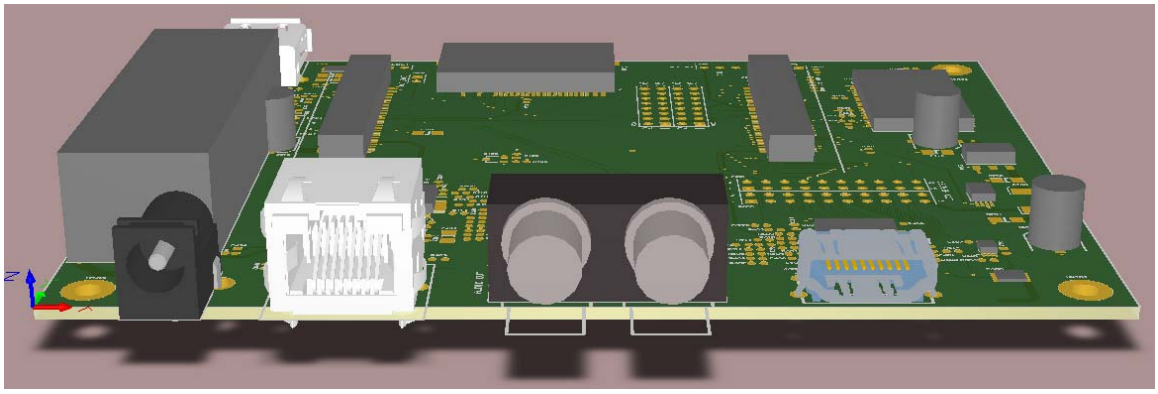

Figure 1-3: KBOC_BB2 3D VIEW FROM FRONT

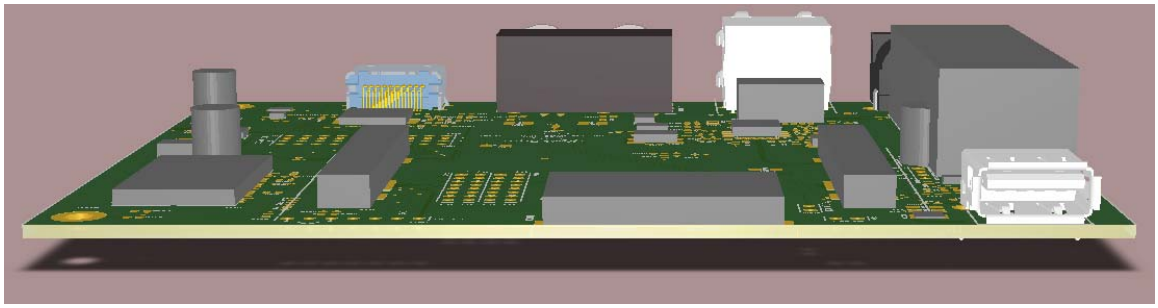

Figure 1-4: KBOC_BB2 3D VIEW FROM BACK

1.2 Connector Location and Pin-Out

The figure below shows the KBOC_BB2 with all connectors and headers labeled.

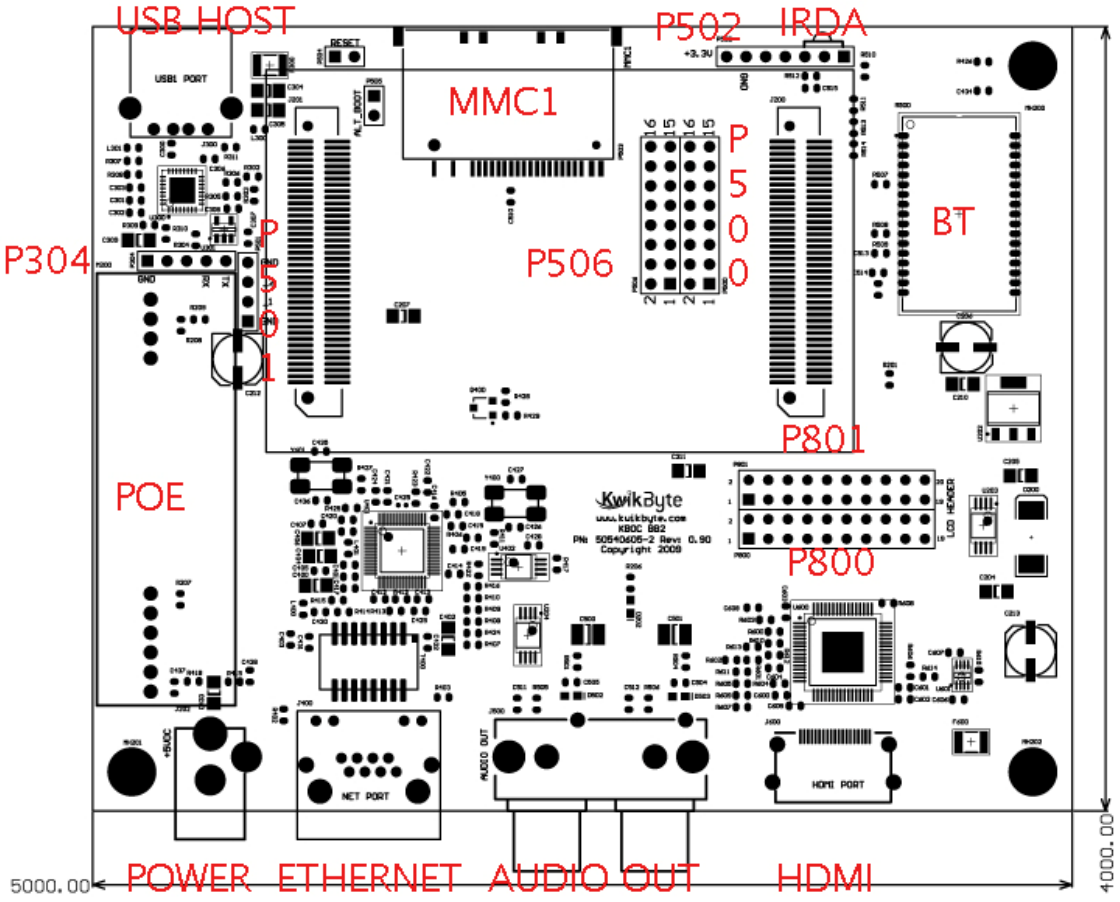

Figure 1-5: KBOC_BB2 CONNECTOR/HEADER LABELS

1.2.1 Connector Description

The list below describes each card-edge connector.

POWER:
Input power supply. Standard 2.1mm barrel jack, center-positive supply must be supplied with +5VDC. Current rating depends on application. This positive supply signal is called “DC_5V”.

ETHERNET:
Standard 10/100Mbps Ethernet jack.

AUDIO-OUT:
Audio output at line level – RCA jacks.

HDMI:
Standard HDMI video output connector (no HDCP).

BT:
Bluetooth module.

IRDA:
Infrared receiver module.

MMC1:
Standard SD/MMC/mini SD/ micro SD connector. Typically used for mass-storage support.

USB HOST:
Standard, type-A USB high-speed host port.

POE:
Power-over-Ethernet supply module.

SERIAL:
The serial connection is available at P304 and intended for use with TTL-232R-3V3 USB/serial adapter cable. The black wire on the cable is plugged-in to the GND pin (nearest the edge of the board). In this configuration, the green pin does not mate with the header.

1.2.2 Header Pin-out

The tables below describe the header pin-out information. The headers are standard, 0.100" x 0.100" through-hole headers that are not populated. This makes soldering to the signals very easy.

PIN	SIGNAL
1	GND
2	NC
3	NC
4	US3_3.3V_RX
5	US3_3.3V_TX

Table 1-1: P304 Pin-out

PIN	SIGNAL
1	GND
2	VIDEO_OUT_1
3	VIDEO_OUT_2
4	GND

Table 1-2: P501 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	US2_RX (MCBSP3_FSX)	AE5
2	GND	
3	+3.3V (through current limit R)	
4	GND	
5	US2_TX (MCBSP3_CLKX)	AF5
6	+3.3V	
7	VIO_1V8	

Table 1-3: P502 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	MCBSP1_FSX	K26
2	MCBSP1_DX	V21
3	MCBSP1_FSR	AA21
4	MCBSP1_CLKX	W21
5	SPI1_SIMO	AB4
6	SPI1_CLK	AB3
7	VIO_1V8	
8	SPI1_CS3	AB2
9	MCBSP3_DX	AF6
10	MCBSP3_FSX (US2_RX)	AE5
11	GND	
12	MMC2_DAT3	AF4
13	MMC2_DAT0	AH5
14	MMC2_DAT2	AG4
15	I2C2_SCL	AF15
16	I2C2_SDA	AE15

Table 1-4: P500 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	MCBSP1_CLKR	Y21
2	GND	
3	MCBSP1_DR	U21
4	MCBSP1_CLKS – N/C	NOT CONNECTED
5	SPI1_SOMI	AA4
6	AUXR	
7	GND	
8	AUXL	
9	MCBSP3_CLKX (US2_TX)	AF5
10	MCBSP3_DR	AE6
11	MMC2_DAT6	AF3
12	MMC2_DAT7	AE3
13	GND	
14	+3.3V	
15	GND	
16	+3.3V	

Table 1-5: P506 Pin-out

PIN	SIGNAL	OMAP35xx BALL
1	DD_HS	D26
2	DD_VS	D27
3	GND	
4	GND	
5	DD0	AG22
6	DD1	AH22
7	DD4	AG24
8	DD5	AH24
9	DD8	F27
10	DD9	G26
11	DD12	AB28
12	DD13	AB27
13	DD16	G25
14	DD17	H27
15	DD20	E28
16	DD21	J26
17	DD22	AC27
18	DD23	AC28
19	DC_5V	
20	DC_5V	

Table 1-6: P800 Pin-out

* All display lines are at +1.8V level.

PIN	SIGNAL	OMAP35xx BALL
1	DD_EN	E27
2	DD_CK	D28
3	+3.3V	
4	VIO_1V8	
5	DD2	AG23
6	DD3	AH23
7	DD6	E26
8	DD7	F28
9	DD10	AD28
10	DD11	AD27
11	DD14	AA28
12	DD15	AA27
13	DD18	H26
14	DD19	H25
15	GND	
16	GND	
17	I2C3_SCL	AF14
18	LCD_PWR_ENn	AE4 (MMC2_DAT4)
19	I2C3_SDA	AG14
20	LCD_PUP	AE2 (MMC2_CLKO)

Table 1-7: P801 Pin-out

1.3 On-Board Signal Routing

The lists below describe signals used on-board.

Ethernet Chip Reset Signal:
Active low reset, +3.3V signal. This is designed for future use and not installed by default.
ETH_RESETn : GPIO150 : W8 : Mode 4 0x2180

USB Hub Reset Signal:
Active low reset, +3.3V signal.
USB_HUB_RESETn = GPIO24 : AE7 : Mode 4 0x25F0

DVI Enable Signal:
Active low reset, +3.3V signal.
DVI_PUP = GPIO170 : J25 : Mode 4 0x216C

LCD Enable Signal:
Driven at +1.8V level to header P801 pin 20. For use as general purpose IO.
LCD_PUP = GPIO130 (MMC2_CLKO) : AE2 : Mode 4 0x2158

LCD Power Enable Signal:
Driven at +1.8V level to header P801 pin 18. For use as general purpose IO.
LCD_PWR_ENn = GPIO136 (MMC2_DAT4) : AE4 : Mode 4 0x2164

Monitor Detect Signals:
Buffered bidirectional signals driven at DC_5V level routed to HDMI connector – also wired at logic level at header 801.
I2C3_SCL = AF14 : Mode 0
I2C3_SDA = AG14 : Mode 0

Serial Channel 3 Signals:
Buffered +3.3V signals wired to header P304.
US3_TX = H21 : Mode 0
US3_RX = H20 : Mode 0