



## KBOCv090: Bottom View

The diagram shows the connector orientation from the bottom view: i.e., looking up at the bottom of the device.

These connectors utilized on the system module (a.k.a. "clip") are FX6-80P-0.8SV. The stacking height of the connectors is an assembly configuration option. Please contact KwikByte if your application requires very small stacking height.

The corresponding connectors utilized on the base board are FX6-80S-0.8SV.

SIGNAL	35xx BALL	J1 PIN	J1 PIN	35xx BALL	SIGNAL
VIO_1V8		1	80		VIO_1V8
VIO_1V8		2	79	J25*	DVI_PUP
DISP_HSYNC	D26	3	78	E27	DISP_EN
DISP_CLK	D28	4	77	D27	DISP_VSYNC
DISP_D8	F27	5	76	E26	DISP_D6
DISP_D9	G26	6	75	F28	DISP_D7
DISP_D20	E28	7	74	J26	DISP_D21
DISP_D18	H26	8	73	H25	DISP_D19
DISP_D16	G25	9	72	H27	DISP_D17
DISP_D11	AD27	10	71	AG22	DISP_D0
DISP_D12	AB28	11	70	AH22	DISP_D1
DISP_D13	AB27	12	69	AG23	DISP_D2
DISP_D14	AA28	13	68	AH23	DISP_D3
DISP_D15	AA27	14	67	AG24	DISP_D4
DISP_D22	AC27	15	66	AH24	DISP_D5
DISP_D23	AC28	16	65	AD28	DISP_D10
VIO_1V8		17	64		VIO_1V8
GND		18	63		GND
I2C3_SCL	AF14	19	62	AG14	I2C3_SDA
US1_TX	AA8	20	61	Y8	U21_RX
MCBSP1_DR	U21	21	60	K26	MCBSP1_FSX
MCBSP1_CLKX	W21	22	59	V21	MCBSP1_DX
MCBSP1_FSR	AA21	23	58	Y21	MCBSP1_CLKR
GND		24	57		GND
SPI1_SIMO	AB4	25	56	AA4	SPI1_SOMI
SPI1_CS3	AB2	26	55	AB3	SPI1_CLK
VIO_1V8		27	54		VIO_1V8
MCBSP3_FSX	AE5	28	53	AE6	MCBSP3_DR
MCBSP3_DX	AF6	29	52	AF5	MCBSP3_CLKX
GND		30	51		GND
MMC2_DAT7	AE3	31	50	AE4	MMC2_DAT4
MMC2_DAT6	AF3	32	49	AE2	MMC2_CLKO
MMC2_DAT3	AF4	33	48	AH3	MMC2_DAT5
MMC2_DAT2	AG4	34	47	AH4	MMC2_DAT1
MMC2_DAT0	AH5	35	46	AG5	MMC2_CMD
N/C		36	45		N/C
N/C		37	44		N/C
N/C		38	43		N/C
I2C2_SDA	AE15	39	42	AF15	I2C2_SCL
GND		40	41		GND

\* = Buffered

SIGNAL	35xx BALL	J2 PIN	J2 PIN	35xx BALL	SIGNAL
DC_5V	INPUT PWR	1	80	INPUT PWR	DC_5V
DC_5V	INPUT PWR	2	79	INPUT PWR	DC_5V
DC_5V	INPUT PWR	3	78	INPUT PWR	DC_5V
GND		4	77		GND
N/C		5	76	R11	USB_OTG_ID
N/C		6	75	T10	USB_OTG_P
N/C		7	74	T11	USB_OTG_N
N/C		8	73		N/C
GND		9	72		N/C
VIDEO_OUT1	Y28	10	71		N/C
VIDEO_OUT2	W28	11	70		N/C
GND		12	69		N/C
VBUS_5V0	R8	13	68		GND
N/C		14	67	B5	HSOR
MICBIAS1	D1	15	66	B4	HSOL
VBAT	A3,C1,B2	16	65	A3,C1,B2	VBAT
MIC.MAIN.P	E2	17	64	G1	AUXR
MIC.MAIN.M	F2	18	63	F1	AUXL
VIO_1V8		19	62		VIO_1V8
VMMC1	K25, C2	20	61	K25, C2	VMMC1
MMC1_DAT4	P27	21	60	P26	MMC1_DAT5
MMC1_DAT3	P28	22	59	N25	MMC1_DAT2
MMC1_DAT1	N26	23	58	M27	MMC1_CMD
MMC1_DAT7	R25	24	57	N27	MMC1_DAT0
MMC1_CD	P12	25	56	R27	MMC1_DAT6
MMC1_WP	AH8	26	55	N28	MMC1_CLKO
3.3V	input source	27	54	input source	3.3V
US3_TX	H21	28	53	H20	US3_RX
GND		29	52		GND
nRESET	AH25*	30	51	AE21	SYS_BOOT5
GND		31	50		GND
LED0_GPIO150	W8	32	49	AA9	LED1_GPIO149
REGEN	A10	33	48	AE7	USB1HS_nRST
GND		34	47		GND
USB1_DAT6	AF13	35	46	AH14	USB1_DAT3
USB1_DAT1	AG12	36	45	AE13	USB1_DAT7
USB1_DAT4	AE11	37	44	AH12	USB1_DAT2
USB1_DAT5	AH9	38	43	AF11	USB1_DAT0
USB1_DIR	AF9	39	42	AG9	USB1_NXT
USB1_CLK	AE10	40	41	AF10	USB1_STP

\* = Buffered from nRESPWRON

**SIG** = Ball listed on TPS659x0 power chip

User must supply +3.3V for correct operation of US3.

US3 signals are at +3.3V level as supplied by 3.3V input pins (2 pins).

VBUS\_5V0 is normally connected to DC\_5V